UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/751,714	01/05/2004	Wing K. Luk	YOR920030603US1	2257

7590 08/04/2006

Ryan, Mason & Lewis, LLP,
Suite 205
1300 Post Road
Fairfield, CT 06824

EXAMINER	
MONDT, JOHANNES P	
ART UNIT	**PAPER NUMBER**
3663	

DATE MAILED: 08/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/751,714	LUK ET AL.	
	Examiner	Art Unit	
	Johannes P. Mondt	3663	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *3-8,17-20,24-28,36 and 37* is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2005* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/22/06 has been entered.

Response to Amendment

Amendment filed 5/22/06 with said RCE forms the basis of this office action. In said Amendment applicant substantially amended claims 1, 3, 4, 6, 16, 21, 22, 24, and all other claims through dependency thereon. Comments on Remarks submitted with said Amendment are included below under "Response to Arguments".

Drawings

In order to avoid abandonment, the drawing informalities noted in the paper mailed on 9/14/05, must now be corrected. Correction can only be effected in the manner set forth in the above noted paper.

1. *Figures 1B, 2B, 4B, 5B, 6, 7, 8 and 9* should be designated by a legend such as --Prior Art-- because only that which is old is illustrated (see page 8, lines 10-18). See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheets should be labeled "Replacement Sheet" in the page header (as per

37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not acceptable to the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. ***Claim 12*** is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim contains subject matter not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. In particular, a gate diode otherwise defined by claim 12 with the source diffusion region abutting the gate and drain diffusion region abutting another side of gate wherein the second terminal is coupled to the source diffusion region and wherein the first terminal is coupled to the gate is not a two-terminal semiconductor device but instead a one-terminal semiconductor device, because source/drain and gate are short-circuited.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. ***Claims 1-2, 9-16, 21-23,and 29-35*** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In particular, the limitation "wherein the two-terminal semiconductor device is adapted to amplify said signal in response to a substantial change in voltage of said control signal" (lines 12-13 of claim 1 and lines 13-15 of claim 21). Said two-terminal semiconductor device is disclosed as gate diode and is in itself not adapted while a function either is there inherently or is not. The newly added limitation thus raises the question whether "adapted" refers to the device or to its function and if to its function whether merely by placement within the integrated circuit.

3. ***Claim 32*** recites the limitation "the step" in line 3. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. ***Claims 1-2, 9-10, 13-15, 21, 23, 31 and 35*** are rejected under 35 U.S.C. 102(b) as being anticipated by Mead et al (5,844,265). With reference to the rejection above under 35 USC 112, second paragraph, examination is carried out assuming "adapted to amplify said signal" means "placed in an environment wherein said signal is amplified"

while no amplifying function other than an inherent one as capacitor (through attraction of charges by a control signal on one of its two terminals leading to a larger voltage change on the other terminal) is assumed involved in any adaptation.

Mead et al teach (title, abstract, Figures 1, 3, 6, 7, and 9; cols. 2-10) a circuit 10 (col. 2, l. 65) for amplifying signals (abstract, first sentence), the circuit comprising:

a control line (LOAD BIAS connected to a bias voltage source) (cf. col. 3, l. 10-20 and Fig. 7); and

a two terminal semiconductor device 62-1 (MOS transistor used as varactor with source and drain short-circuited: col. 3, l. 33-43; cf. Fig. 1, 9 included as 62-1, 62-2, in Fig. 7), having first and second terminals (loc.cit.), the first terminal (gate of gated diode 62-2) coupled to a signal line 194-1 (of sense amplifier 10), and the second terminal coupled to the control line (capacitively, through 16-1) (loc.cit.), wherein the two terminal semiconductor device is adapted to have a capacitance (gate-channel/source/drain capacitance) when a voltage on the first terminal relative to the second terminal is in a first voltage range and to have a lower capacitance when the voltage on the first terminal relative to the second terminal is in a second voltage range (because the MOS varactor = gated diode inherently has a variable capacitor, wherein the gate voltage can be raised or lowered (depending on the conductivity type of the varactor) to cause depletion, and even further to cause inversion of the channel),

wherein the control line is adapted to be coupled to a control signal (through the capacitive coupling to the aforementioned bias voltage source); and

wherein the signal line is adapted to be coupled to a signal (from the vertical scanner) and to be an output of the circuit (through 218) (col. 8, l. 44-col. 9, l. 64), and wherein the two-terminal semiconductor device is CAPABLE of amplifying said signal in response to a substantial change in voltage of said control signal: by admission by applicant, Figure 11A of disclosure: any amplifying function must be across the node of 1101/1110 and hence is inherent as a property of *capability* of said gate diode. In reference to the claim language referring to ""wherein the two-terminal semiconductor device is adapted to amplify", intended use and other types of functional language must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim. In re Casey,152 USPQ 235 (CCPA 1967); In re Otto , 136 USPQ 458, 459 (CCPA 1963).

Finally, the limitation "adapted" pertains itself to a method of making the device and as such constitutes a product-by-process limitation. The limitation "adapted" is only of patentable weight in as much as the method steps distinguish the final structure, and to the extent not impacting final structure are taken to be product-by-process limitations and non-limiting. A product by process claim is directed to the product per se, no matter how they are actually made. See In re Fessman, 180 USPQ 324, 326 (CCPA 1974); In re Marosi et al, 218 USPQ 289, 292 (Fed. Cir. 1983), and In re Thorpe, 227 USPQ 964, 966 (Fed. Cir. 1985), all of which make clear that it is the patentability of the final structure of the product "gleaned" from the process steps that must be determined in a "product-by-process" claim, and not the patentability of the process. See also MPEP

2113. Moreover, an old or obvious product produced by a new method is not a patentable product, whether claimed in "product by process" claims or not.

On claim 2: the two terminal semiconductor device by Mead et al comprises a gated diode 62-1 (also 32 in Fig. 1) (Fig. 7) having a well (N.B.: substrate is a p-well; col. 5, l. 1-5; Fig. 3) because it is implemented as p-type substrate 156 (Fig. 6 and col. 7, l. 65) in Fig. 6, which inherently is a (electrostatic potential) well for all majority charge carriers therein) and wherein the threshold voltage can inherently be modified by modifying a dopant level in said well of the gated diode because said dopant level determines the number of charge carriers (see, for instance, Wolf, ISBN 0-961672-5-3, pages 116-133).

On claim 9: the circuit further comprises an output circuit 206-1 / 216 (Fig.7) adapted to produce an output corresponding to a voltage at the gate input of the gated diode (depending as it is on the capacitance of capacitor 62-1).

On claim 10: the output circuit comprises one or more of the following: a buffer, an inverter, and a latch, because the hold/sample circuit 206 (col. 9, l. 25-32) is a buffer circuit.

On claim 13: the two terminal semiconductor device comprises a gated diode 32 (62-1, 62-2) (col. 3, l. 33-43) (N.B.: source and drain both connected to the output of the sense amplifier and hence also to each other, forming one pole of the diode, the gate forming the other one).

On claims 14-15: the gated diode is an n-type gated diode (col. 3, l. 36) or a p-type gated diode (col. 3, l. 33-35), wherein the threshold voltage is a positive,

respectively negative voltage (inherently, a positive voltage is required to cause inversion in the former, a negative voltage in the latter, wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal relative to the second terminal is more positive, respectively negative, than the threshold voltage and to have a lower capacitance when the voltage on the first terminal is less positive, respectively negative, than the threshold voltage.

On claim 21: Mead et al teach a method for amplifying signals (cf. title), the method comprising the steps of: determining that a voltage on a signal line 194-1 (Fig. 7) is to be amplified (any voltage on input line 194-1 meets the claim limitation); and modifying voltage on a control line (LOAD BIAS) (by biasing the LOAD BIAS) (Fig. 7), wherein the control line is coupled to a second terminal (gate of 62-1) of a two terminal semiconductor device 62-2 (Fig. 7), the two terminal semiconductor device having the second terminal and a first terminal, the first terminal (terminal connected to both source and drain of MOSFET 62-1 (col. 3, l. 33-43) coupled to the signal line, the second terminal coupled to the control line (loc.cit.), wherein the two terminal semiconductor device is adapted to have a capacitance when a voltage on the first terminal is in a first voltage range and to have a lower capacitance when the voltage on the first terminal is in a second voltage range (such adaptation, given the selection of a MOSFET for said two-terminal device, with source and drain directly connected, is unnecessary but instead it is inherent, given the creation of an inversion layer for sufficiently positively large or sufficiently negatively large enough voltage; it is also specifically cited as said device is a varactor, i.e., variable capacitor: see col. 3, l. 27-43)) and wherein the control

line is adapted to be coupled to a control signal (LOAD BIAS; loc.cit.) and wherein the signal line is adapted to be coupled to a signal (through photo-sensor 184-1) and to be an output 218 of the circuit (col. 9, l. 54-64); and

wherein the signal line is adapted to be coupled to a signal (from the vertical scanner) and to be an output of the circuit (through 218) (col. 8, l. 44-col. 9, l. 64), and wherein the two-terminal semiconductor device is CAPABLE of amplifying said signal in response to a substantial change in voltage of said control signal (by admission by applicant, Figure 11A of disclosure: any amplifying function must be across the node of 1101/1110 and hence is inherent as a property of capability of said gate diode).

On claim 23: the two terminal semiconductor device comprises a gated diode (MOSFET with source and drain directly interconnected is a gated diode) (col. 3, l. 33-43) having a well (p-type substrate is an electrostatic well for charge carriers) (N.B.: substrate is a p-well; col. 5, l. 1-5; Fig. 3) and wherein, inherently, the threshold voltage can be modified by modifying a dopant level in the well of the gated diode: the more dopant available, the higher the charge in the capacitor can become).

On claim 31: the two-terminal device comprises a gated diode 62-1 (cf. Fig. 7 and col. 3, l. 33-43).

On claim 35: the method further comprises the step of determining an output corresponding to the signal (inherently so, because output inherently is looked at and hence determined).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. ***Claim 11*** is rejected under 35 U.S.C. 103(a) as being unpatentable over Mead et al as applied to claim 1, and in view of Ravi et al (US 2004/0263272 A1) and Brachitta et al (6,130,469).As detailed above, Mead et al anticipate claim 1. Mead et al do not teach the further limitation defined by claim 11 as a whole although they clearly teach a MOS n-channel transistor as the basis for their varactor 32, which inherently has an insulation formed between the gate and the well and a source region (see col. 3, l. 33-43), and although they clearly teach the first terminal is coupled to the gate and the second terminal is coupled to the source (see above, discussion of claim 1).

However, it would have been obvious to include said further limitation on overlapping of said source region "one side of the insulator and gate" in view of Ravi et al, who teach said overlap in a varactor to be non-zero so as to have a minimum capacitance in the OFF state (see [0066]). *Motivation* to include the teaching by Ravi et al derives from the resulting improved controllability of the ratios of capacitances in OFF and ON state in the varactor so as to have a more accurately quantified varactor.

Furthermore, it would have been obvious to include the limitation "a shallow trench isolation region abutting another side of the insulator and gate" in view of Brachitta et al,

who teach said STI region to insulate MOS capacitors from neighboring FET devices (col. 2, l. 13-23) thus making the devices independent as they should. *Motivation* to include the teaching by Brachitta et al in the invention by Mead et al derives from said advantage of device independence coupled with the presence in one wafer of several FETs and the varactor as MOS capacitor also in Mead et al (32 is varactor as MOS capacitor in wafer with FETs (col. 7, l. 3-36).

Response to Arguments

Applicant's arguments filed 5/22/06 have been fully considered but they are not persuasive.

On the Drawings: applicants' traverse of objection 1 does not address the specific quotes from applicants' own specification admitting the prior art nature of the drawings, as explained in detail in the previous office action. Therefore, the objection stands. Drawing objection 2 (relating to claim 22) is withdrawn in light of applicants' comments.

On claims 3 and 24: they are held allowable in light of said amendment.

On claims 1, 3, 4, 6, 16, 21, 22 and 24: Applicants' comments are not understood: there is no trace of four voltage ranges in claim 1 nor in claim 21. Newly added limitations introduce indefiniteness as noted and explained above under 35 USC 112, second paragraph.

Prio Art Rejections:

Applicants allege that "the varactors (62-n) of Mead are not even used for signal amplification" (page 14 of Remarks). However, the two terminals of said varactors are

the input and output terminals between which amplification takes place (see also Figure 1 and discussion, input and output being 18 and 28, and the varactor being 32). Furthermore, specific function only has patentable weight in as far as the device is capable of performing the function, and as such there is no doubt in light of the amplification that admittedly takes place in applicant's configuration, which must take place between the nodes of 1101 and 1110 in Figure 11A; the function itself constitutes, when claimed, functional language, and applicant refers to the case law cited above to explain why this function itself is not of any patentable weight. Applicants also suggest Mead's varactors are not two-terminal devices, which is not at all persuasive: see Figure 1 and description, especially the short-circuit as clearly indicated in Figure 1, between source and drain).

Applicants further argue that 62-1 of Mead et al are not coupled to a control line, which is incorrect, as witnessed by the LOAD bias controlling the voltage source of the varactors 62-n (see Figure 7).

Applicants further argue that Mead et al do not disclose that the varactor is adapted to amplify a signal. First, the process of adaptation itself has no patentable weight in the product invention while only the capability of performing an amplification function is of patentable weight, not the amplification process itself, in as far as claim 1 is concerned.

Second, said two-terminal semiconductor device is disclosed as gate diode and is in itself not adapted while a function either is there inherently or is not. The newly

added limitation thus raises the question whether "adapted" refers to the device or to its function and if to its function whether merely by placement within the integrated circuit.

Thus is suffice to point out, as done in detail above, that the substantial change in voltage of the control signal is a capability of the device.

Parenthetically, a varactor in the form of a MOS capacitor has symmetric functionality in that poles could be reversed in their roles, because it is a capacitor.

Finally, further search has revealed art against claim 11 while "abutting" og source region and gate appears implied by the present formulation of claim 12, but in that case the two-terminal device cannot operate as such, the terminals being short-circuited, whence the above rejection for lack of enablement, of claim 12.

The above rejections were prompted by these considerations.

Allowable Subject Matter

2. ***Claims 3-8, 17-20, 24-28 and 36-37***are allowed. Closest art found to date is Mead et al, however, there is no isolation device between the signal line 194-1 and the two-terminal semiconductor device (varactor) 62-n.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Kudo (3,805,176) (entire document, especially col. 1, l. 20-32 and col., 4, l. 6-21).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Johannes P. Mondt whose telephone number is 571-272-1919. The examiner can normally be reached on 8:00 - 18:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack W. Keith can be reached on 571-272-6878. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JPM
August 2, 2006

Patent Examiner:

Johannes Mondt (Art Unit: 3663)